EEPROM Reliability

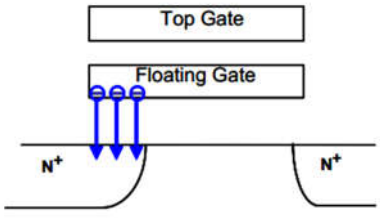
A portion of IC products supplied and clock products manufactured by VC America are calibrated to achieve tight or high stability performance as low as 3ppm (all inclusive). Products include High Stability CMOS clocks and some RTC [real time clocks] and 32.768 kHz output devices. Units are calibrated at VC America and verified over temperature. Product reliability is confirmed with industry standard mechanical and electrical tests including dynamic burn-in and HTOL [High Temperature Operating Life] testing[1].

These devices use a small number of EEPROM cell (bits) to store calibration values.

Non-volatile memory products incorporating EEPROM and FLASH memory have application specific needs for higher density and lower cost. This drives manufacturers to develop products with reduced memory cell size via smaller feature sizes and new design architectures. Implementation of advanced cell designs and architectures have transitioned memory cell design from SBC [Single Bit per Cell designs with separate read, write, and erase functions to MBC [Multiple Bit per Cell] with shared bit channel erase functions, and migration to fine line geometries ≤65nm. Flash memory architectures include error block correction and wear leveling to improve memory performance while achieving greater densities; excellent for intended applications despite introduction of additional failure mechanisms not evident in larger geometry SBC EEPROM. Some of these failure mechanisms include data loss at <150°C, adjacent cell interaction, de-trapping (1.1eV), and SILC [Stress Induced Leakage Current <0eV].

JEDEC JESD47 data retention revisions moved from initial stress-test-driven requirements (time, temperatures, sample sizes) to include new dominant failure mechanisms, a sliding scale for data retention with 10 years for lower cycle counts and 1 year for max-specification cycle count, and considerations for high density counts and comprehending error [block] correction and wear leveling.

[VC America calibrated products using EEPROM design are simple products with Single Bit per Cell (SBC) architecture and ~350nm technology, with a small number of stand-alone bits with single charge loss mechanism. EEPROM cell structure consists of three transistors: one for READ, WRITE, and erase. WRITE and erase use Fowler-Nordheim tunneling methods through a floating thin gate.



[1] . High reliability mission critical applications include screening per JPL 2005 Final Report-MNOS EEPROM. (min bake 78hrs@150°C in 0101 and reversed 1010 states)

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Two failure modes of EEPROM cells[2]

- Endurance: WRITE cycles trap electrons in the floating gate and reduce voltages of logic levels (zero and one); eventually to the point logic states are not readable.
- Data retention: Time and temperature allow drift or dissipation of electrons through the dielectric insulator. This is more acute at increased temperatures. The result is changing cell to an erased state.

Clock products using EEPROM are calibrated and then verified at temperature points. Products specified for -55°C to 125°C are verified in 5°C steps from -55°C to 125°C.

- EEPROM registers are written during calibration.
- EEPROMs are not written during use in application.

Operation of clock oscillators over their lifetime requires EEPROM read only. For this type product and application usage, EEPROM data retention is the primary failure mechanism.

To determine VC America's HSD/HSXO and related EEPROM products exhibit acceptable data retention for high temperature operation, we devised an extreme temperature test.

Test goals

1. Determine EEPROM Data Retention for Total life, MTTF, FIT, Reliability
2. Confirm Data Retention for device operation to 125°C
3. Conduct test for Data Retention to assess higher temperature operation to 200°C
4. Calculate EEPROM cell activation energy for READ only condition for our products
5. Confirm results are consistent with from JPL 2005 Final Report-MNOS EEPROM recommendations

Data Retention Test Summary

Following results based on 3500 hours completed. All 200 units in bakes successfully read and match initial 0 hour read values. There is substantial detail in the following pages, however, this summarizes results.

A. MTTF of >459,000 YEARS @ 55°C operating temperature exceeds requirements
B. Results at 250°C demonstrate suitability for 125°C applications
C. Results at 250°C and 295° demonstrate suitability for > 125°C applications
D. 0 failures from both lots thwarts direct calculation [and upward revision] of activation energy Ea using planned method.
E. Survival of all units at this point is unexpected (excellent) event.
F. Additional screening recommendations of JPL 2005 Final Report – MNOS EPPROM regarded as adequate screen for high reliability and mission critical applications.

[2] EEPROM calibration data loss degrades frequency stability; devices remain functional.

Data Retention Test[3]

To test EEPROM data retention, we employ use of high temperature accelerated tests on HSxx series clocks and the Arrhenius Law equation which predict device behavior under normal operating conditions from results testing devices at accelerated temperatures for shorter periods of time.

What is the activation energy for non-volatile memory used in our products? The reliability group determine IC process activation energy rating as Ea=0.69eV (all modes combined). Older industry reliability reports and studies for EEPROM single-bit-per-cell structures with independent WRITE and READ have used a "generally accepted" activation energy of Ea = 0.60 eV. At least one manufacturer established Ea = 0.80 eV. The Ea assumes continued WRITE and READ operation over its life, where EEPROM endurance is the primary failure mechanism.

Data retention is the primary failure mechanism. EEPROM is READ only for its entire useful life, after a small [<100] number of WRITEs during calibration. We found no study of data retention on EEPROM cells programmed a small [<100] number of times, however, JESD47 include a sliding scale for data retention with 10 years for lower cycle counts and 1 year for max-specification cycle count.

Data retention activation energy (Ea) coefficients of EEPROM programmed a limited number of times may differ from EEPROM continually written and read throughout its useful life. We use the activation energy of Ea=0.60eV as starting point in our calculations. Further, we conduct test at two stress levels to point of failure and re-calculate EEPROM cell activation energy for READ only operation.

Devices used during test are calibrated with register values read and written to different values. Devices are read prior to bake and periodically devices removed from ovens and EEPROMs are read and returned to bake. A failure occurs when any cell changes logic state values or cannot be read. Two temperatures used for baking are 250°C and 295°C.

Test Plan

1. Devices from Standard production
2. Calibrate devices through two temperature cycles (In production, one cycle is typical)
3. Bake 200 units of HSxx series at high temperature
4. Bake 100 units each at 250°C and 295°C.
5. Each 100 unit group consists of 50 each of from 2 different lots and frequencies.
6. Serialize units and read EEPROM registers prior to bake.
7. Periodically remove units from bake, read EEPROM registers, and return to the ovens.

[3] We are pleased to acknowledge the wealth of existing prior work by industry contributors on reliability methods and calculations, and of non-volatile memory construction and failure modes, which are referenced at end and are integral part of this report.

8. Reliability calculations made
    a. Standard reliability calculations @ 55°C as the average operating temperature for the device specified for operation over -55°C to 125°C.
    b. Mission Critical applications use higher confidence levels for FIT and MTBF/ MTTF calculations as well as higher average operating temperatures
    c. Include a Matrix of junction temperature and confidence level calculations.

Test Groups

Temperature	Group 1 @ 250°C	Group 2 @ 295°C	Total
Lot 1 (15MHz)	50	50	100
Lot 2 (38.8MHz)	50	50	100
Total	100	100	200

Risks conducting accelerated data retention test:

Testing conducted in this study focus on overall reliability of the EEPROM used to calibrate our products, and establish data retention characteristics achieve acceptable device useful life (MTTF, MTBF) for use in high reliability and high temperature applications.

Units selected are standard production consisting of ceramic LCC, semiconductor IC attached with adhesive, interconnected to package pads using gold wire wedge bonding, and adhesive mounted quartz crystal. Units are hermetically seam-sealed (welded) with nickel plated KOVAR lid. Potential failures to read EEPROM during test not attributable to the IC include:

Wire bond failure at IC pads exposed for long times at elevated temperatures.
Adhesive: Out-gassing and material degradation lead to failure and higher crystal aging.

A device failure occurs when EEPROM READ register values differ from initial values or cannot be read, or if device fails to function. At time of failure, failed unit(s) will be confirmed unreadable by bench fixtures. FA (failure analysis) is required to determine root cause.

Bake Test EEPROM read results

Total Bake Hours	Group 1 @ 250°C		Group 2@ 295°C	
	Lot 1	Lot 2	Lot 1	Lot 2
0	Pass	Pass	Pass	Pass
500	Pass	Pass	Pass	Pass
1000	Pass	Pass	Pass	Pass
2000	Pass	Pass	Pass	Pass
3000	Pass	Pass	Pass	Pass
3500	Pass	Pass	Pass	Pass

Reliability Calculations

Acceleration Factor AF is result calculated from accelerated life test using Arrhenius equation:

$$AF = e^{-\frac{Ea}{k} \times \left(\frac{1}{T2} - \frac{1}{T1}\right)}$$

Where:

Ea = Activation energy (0.60 eV for data retention)[4]

k = Boltzmann's constant (8.617E-05 eV/K)

T1= Application junction Temperature (Tj) expressed in Kelvin[5]

T2= Accelerated stress junction temperature in Kelvin[6]

K = Absolute zero Kelvin (0°K) =273.15°C

For Tj= 55°C, $AF=e^{-\frac{Ea}{k} \times \left(\frac{1}{(273.15+250)} - \frac{1}{(273.15+60)}\right)} = 2722$

Acceleration Factor AF *		Bake Temperature °C	
		250	295
Tj Junction Temperature	55°C	2722	7812
	85°C	460	1321
	105°C	165	472

* Calculated from Bake Temp and Tj using Arrhenius Law

[4] Device activation energy for HSxx product (Ea) is 0.69. We start using Ea = 0.60 as a generally accepted value for non volatile memory cells for Arrhenius law calculations.

[5] 55°C used as average temperature for -55°C to 125°C rated product, however mission critical applications many use 55°C or temperatures to 125°C application and expected environment.

[6] Baking temperature expressed in degrees Kelvin

Data Retention (years) calculation.

Data retention in years is the baking hours times the Acceleration factor (AF), divided by the number of hours per year.

Data retention (years @ 55°C) = $\frac{(Hours \times AF)}{(Hours\ per\ Year)}$

Days per year = 365.256366 (one rotational orbit around the sun)
Hours per year = 24 x 365.256366 = 8766.1528

Ex: Data retention (years@55°C)= $\frac{(Hours \times AF)}{(Hours\ per\ Year)} = \frac{(3500 \times 3119)}{(24x365.256366)}$ = 1245 Years

Data Retention Years		Bake Temp	
		250°C	295°C
		3500	3500
Tj Junction Temperature	55°C	1086.8	3119
	85°C	183.7	527.4
	105°C	65.9	188.5

Bake Hours x AF divided by hours per year

FIT or Failure-In-Time rate is a measure of failure rate in 10^9 (per billion) hours or quantity of units failed after 10^9 (per billion) hours. It is inversely proportional to number of devices tested.

$$\text{FIT} = \frac{(\chi^2/2)\times 10^9}{N\times H\times AF}$$

N = Number of units H = Bake time in hours

$\chi^2/2$ calculation is excel function CHIINV((100%-CL), deg_freedom)

Rejects R =0
Deg_freedom = 2*R+2 = 2

Confidence level CL=	$Chi^2/2 = X^2/2$ =
60%	0.9163
90%	2.3026
95%	2.9957

Example: 250°C @ 60% CL.

$$\text{FIT: } = \frac{(\chi^2/2)\times 10^9}{N\times H\times AF} = \frac{(0.9163)\times 10^9}{100\times 3500\times 2722} = 0.96$$

Each Lot Size= 100		FIT Failure in Time at Confidence Level CL (3500 Bake Hours)								
		Standard Reliability			Higher Temp			Mission Critical		
FIT (per Billion)		Tj =55°C			Tj=85°C			Tj=105°C		
		250°C	295°C	Combined	250°C	295°C	Combined	250°C	295°C	Combined
CL=	60%	0.96	0.34	0.25	5.69	1.98	1.47	15.87	5.55	4.11
	90%	2.42	0.84	0.62	14.30	4.98	3.69	39.87	13.94	10.33
	95%	3.14	1.10	0.81	18.61	6.48	4.81	51.87	18.13	13.44

[i] **$MTTF_{YEARS}$.** Mean-time-to-failure is the inverse of **FIT** and multiplied by 10^9 (a billion)

$$\mathbf{MTTF_{YEARS}} = \frac{1}{FIT \times 24 \times 365.256366} \times 10^9$$

Each Lot Size= 100		MTTF - Mean time to Failure @ Confidence level CL (3500 Bake Hours)								
		Standard Reliability			Higher Temp			Mission Critical		
MTTF (Years)		Tj =55°C			Tj=85°C			Tj=105°C		
		250°C	295°C	Combined	250°C	295°C	Combined	250°C	295°C	Combined
CL=	60%	118,607	340,395	459,002	20,044	57,560	77,604	7,190	20,567	27,756
	90%	47,199	135,457	182,656	7,976	22,906	30,882	2,861	8,184	11,045
	95%	36,278	104,117	140,396	6,131	17,606	23,737	2,199	6,291	8,490

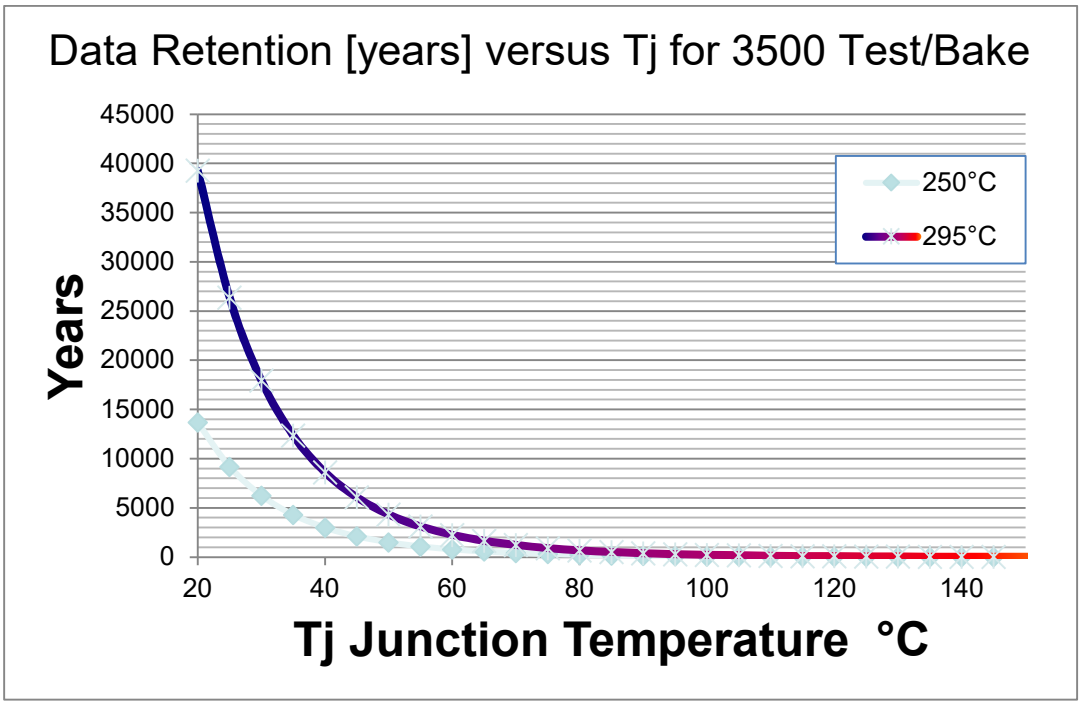
Reliability over a fixed period of time

$$R(t) = e^{-t/MTTF}$$

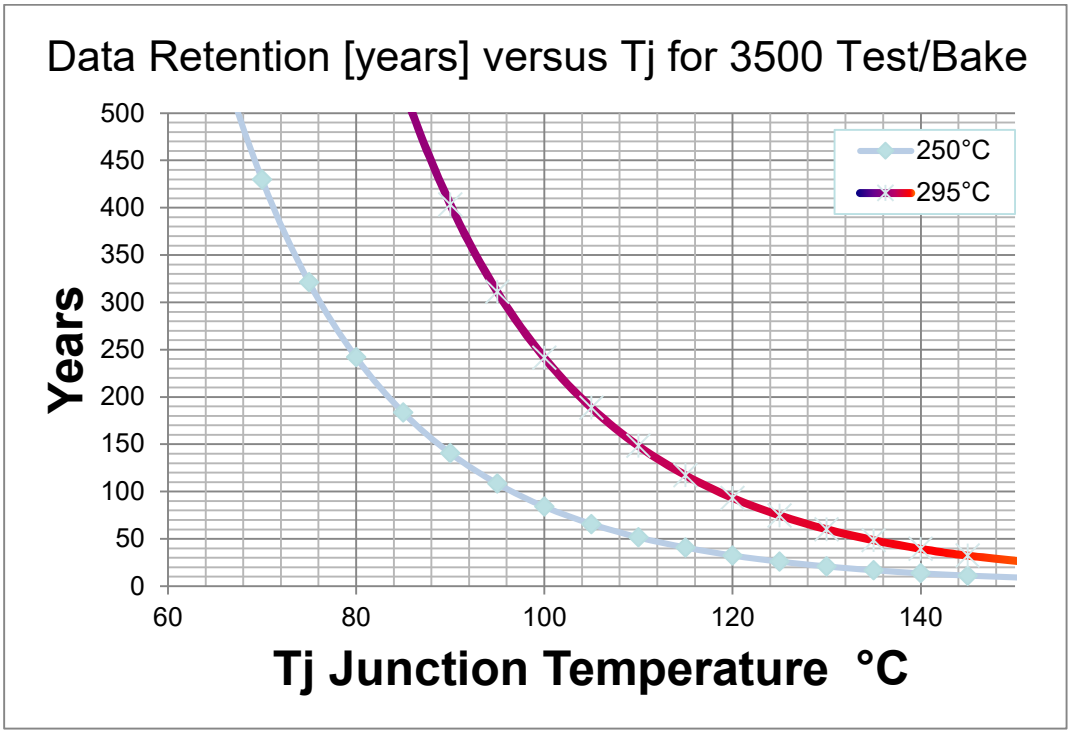
Where t = Fixed Time [years]

Each Lot Size= 100		Reliability over Specified Time (Years) @ Confidence CL (3500 Bake Hours)								
		Standard Reliability			Higher Temp			Mission Critical		
Time (Years) 40		Tj =55°C			Tj=85°C			Tj=105°C		
		250°C	295°C	Combined	250°C	295°C	Combined	250°C	295°C	Combined
CL=	60%	99.966%	99.988%	99.991%	99.801%	99.931%	99.948%	99.445%	99.806%	99.856%
	90%	99.915%	99.970%	99.978%	99.500%	99.826%	99.871%	98.612%	99.512%	99.639%
	95%	99.890%	99.962%	99.972%	99.350%	99.773%	99.832%	98.197%	99.366%	99.530%

Standard Reliability Calculation



Zoom in closer (below)



Data Retention at various operating Junction Temperatures

Data Retention [years] versus Tj for 3500 Test/Bake hours				
Temperature (°C)	250°C		295°C	
	AF	Years	AF	Years
20	34288	13690	98395	39286
25	23023	9192	66067	26378
30	15663	6254	44947	17946
35	10790	4308	30963	12362
40	7522	3003	21585	8618
45	5303	2117	15219	6076
50	3780	1509	10847	4331
55	2722	1087	7812	3119
60	1980	791	5681	2268
65	1453	580	4171	1665
70	1077	430	3090	1234
75	805	321	2309	922
80	606	242	1739	694
85	460	184	1321	527
90	352	141	1011	404
95	271	108	779	311
100	211	84	605	242
105	165	66	472	189
110	129	52	371	148
115	102	41	294	117
120	82	33	234	93
125	65	26	187	75
130	53	21	151	60
135	43	17	122	49
140	35	14	99	40
145	28	11	81	32
155	19	8	55	22
160	16	6	46	18
165	13	5	38	15
170	11	4.4	32	13
175	9.3	3.7	26.6	10.6
180	7.8	3.1	22.4	8.9
185	6.6	2.6	19	7.6
190	5.6	2.2	16.1	6.4
195	4.8	1.9	13.7	5.5
200	4.1	1.6	11.7	4.7
Operating Junction Temperatures used in Report				

Semiconductor Reliability and Failure Mechanisms

The reliability of semiconductor devices varies on their ability to withstand stresses applied to the devices, electrical, thermal, mechanical, and environmental (humidity, pressure, etc). Devices with weak structure(s) by design and/or process result in failures. Design and process rules are established to produce devices capable of functioning under various conditions.

The semiconductor chip, its package construction, manufacturing method and standard and conditions of the device conditions of use are factors which determine useful lifetime and reliability performance.

Electrical load (voltage and current), ESD (static electricity)
Temperature, Humidity, Mechanical stress
Cycling of stress; temperature, humidity, pressure, mechanical, electrical

Standard tests provide a baseline and measure of reliability.

Semiconductor reliability prediction methodologies such as MIL-HDBK-217 use acceleration models. Coefficients of acceleration models are built from empirical data to establish the activation energy used in the Arrhenius law model for temperature acceleration. There is much data that support that Arrhenius Law general formula expressing chemical reaction rate can be used for calculation of the failure rate of semiconductors.

Failure mechanisms recognized in semiconductor and their activation energy range shown below [7][12]:

Failure Mechanism	Activation Energy	Screening and Testing Methodology	Control Methodology
Oxide Defects	0.3 –1.15 eV	High Temperature operating life (HTOL) and voltage stress	SPC (statistical process control) of oxide parameter, defect density control, and voltage stress testing
Silicon defects (Bulk)	0.3 – 0.5 eV	HTOL and Voltage stress screening	Vendor SPC and quality control and of thermal processes
Corrosion	0.45 eV	Highly Accelerated Stress Testing (HAST)	Passivation and dopant control, hermetic sealing control, product handling.
Assembly Defects	0.5 – 0.7 eV	Temperature cycling, temperature & mechanical shock, environmental stressing	Vendor SPC and quality control and of assembly processes proper handling.
Electro-migration -Al trace/line -Contact/ via	 0.6– 0.7 eV 0.9 eV	Test device characterization at highly elevated temperatures	Design process groundrules to match measured data, statistical control of metals, photoresist ,and passivation
Mask and Photoresist Defects	0.7eV	Mask Fab comparison, print check, defect density monitor, voltage stress & HTOL	Clean room control, mask cleaning, pellicles, SPC or photoresist and etch processes
Contamination	1.0 eV	C-V stress of oxides, wafer Fab device stress and HTOL	SPC of C-V data, oxide/interconnect cleans, high integrity glassiviation and clean assembly process
Charge Injection	1.3 eV	HTOL and oxide characterization	Design groundrules based on test results, wafer level SPC of gate length and gate oxide thickness controls.
Data Retention (EEPROM)	0.60-1.15 eV	High Temperature Bake	SPC (statistical process control) of oxide parameter, defect density control, and voltage stress testing for Oxide Defects and quality control of Bulk Silicon growth and thermal processes (optional epitaxial layer)
Endurance (EEPROM)	0.60-0.80 eV	Write and Read to specified count and High temperature Bake	

Generally, lower activation energy factors dominate results (Arrhenius Law models).

Defects of oxide, silicon, mask, and photoresist are random defects screened during initial test or as early life (infant mortality) failures are screened during burn-in testing.

Semiconductor process control and improved defect densities reduce random failure and increase activation energy factors for their failure mechanisms.

Electro-migration is the primary mechanism for failure in most semiconductors.

Specific device structures and circuit elements may have specific failure mechanisms; non-volatile EEPROM and Flash memory are some examples.

Endurance of WRITE cycles and Data retention are specific failure mechanisms of non volatile memory.

Reliability Testing for Semiconductors

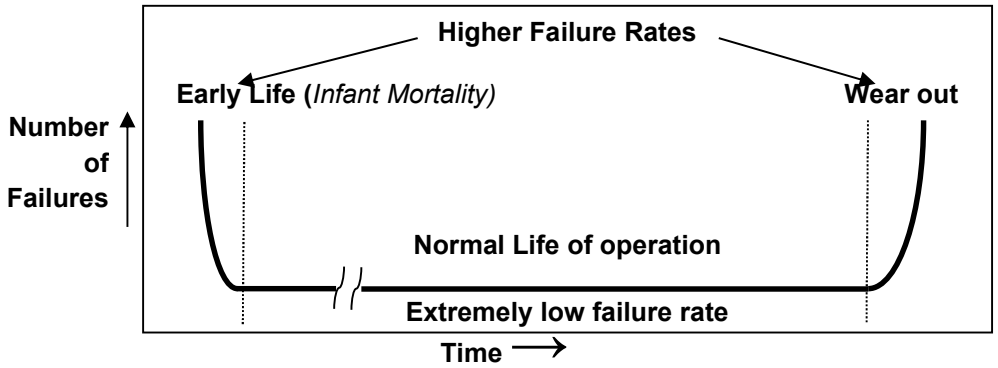
Early life failures or “infant mortality” of semiconductors is generally represented by the bathtub curve below. To reduce failures and increase the reliablity of a population of devices, accelerated burn-in of units is common method to eliminate failures due to random defects, and once removed from the population, the remaining units will exhibit extremely low failure rate until they approach the wear out phase.

Three phases of lifetime: The “bathtub curve” below illustrate represent the failure of devices over their lifetime.

Early life – declining failure rate where failures are attributed to random defects – also referred to as “Infant Mortality”.

Useful or normal life – a steady state period where failure rate is relatively low and constant

Wear out – phase where end of life mechanisms start to occur and failure rate increases



Infant Mortality Screening (During Production). Normal production devices are baked for minimum of 96 hours at 170°C to screen out failures attributed to random defects. For other than data retention mechanisms, burn-In of units for 168 hours @125°C (Mil-Std-883B) is recommended.

Definitions:

Arrhenius equation (for reliability): ***An equation used*** to calculate thermal acceleration factors for semiconductor device ***time-to-***failure ***distributions:***

$$AF = e^{-\frac{Ea}{k}} \times \left(\frac{1}{T2} - \frac{1}{T1}\right)$$

AF is the thermal acceleration factor between temperatures; (JEDEC symbol is AT, we use AF)

E_a is the activation energy (eV); (JEDEC use E_{aa} as the apparent activation energy" [eV]).

- "Apparent activation energy" is derived from observations made by accelerating equal groups at different temperatures to the time of failure (t_f), and then calculating the apparent activation energy. Ea is more commonly used, we defer to using Ea in most formulas.

k is Boltzmann's constant (8.617×10^{-5} eV/K);

T_1 is the absolute temperature of the test (K);

T_2 is the absolute temperature of the system (K).

Operating junction temperature (T_J °C) converted to Kelvin $T_2 = T_J + 273.15$

Acceleration Factor (AF)

AF (JEDEC uses symbol A_T) is result of an accelerated life test performed to predict its long-term performance. It is used in the Arrhenius Law equation. This factor also is an inverse of FIT.

CHI-square (χ^2)

In probability theory and statistics, the **chi-square** distribution $\chi^2(\alpha, \nu)$ where:

α (alpha) probability or CL, and is the percent under the χ^2 probability distribution curve

v(nu) degrees of freedom (distribution of a sum of the squares of v(nu) independent standard normal random variables.)

We use the MS Excel function CHIIINV (probability, deg_freedom) to calculate χ^2, however, this function calculates the right side of the distribution curve; we need the left side. So, for probability is= 1- α or 1-CL and we calculate CHIINV (1-CL, deg_freedom)

v(nu) or deg_freedom is 2R+2 where R = number of rejects or failures

Confidence Level (CL)

CL is the probability level estimated based on sample tests conducted for failures and is a confidence in the integrity of numbers used to determine the sample rate. It follows chi-square (χ^2) distribution and depends on the number of failures. In most cases confidence level is chosen to be 60% however high reliabilty and mission critical uses may be calculated at CL= 90% or 95%.

Failure Rate

Failure Rate (λ) is the number of failures per unit time. It follows the bathtub curve.

Failure-in-Time (FIT) Rate.

FIT is a direct measue of failure rate in 10^9 device hours or the number of devices that failed after 10^9 hours. It is inversely proporational to the number of devices tested and duration of the tests.

$$\text{FIT} = \frac{(\chi^2\ /2) \times 10^9}{N \times H \times AF}$$

χ^2 = Chi-square
N= Number of Units
H = Total Hours

Failure-in-Time (FIT) Rate. FIT is a direct measue of failure rate in 10^9 device hours or the number of devices that failed after 10^9 hours. It is inversely proporational to the number of devices tested and the duration of the tests.

Mean Time to Failure (MTTF). MTTF is the inverse of FIT for a non-repairable device.

Mean Time to Repair (MTTR). MTTR is the time required to complete repairs to a device.

Mean Time between Failures (MTBF). MTBF is the time to failure plus time to repair (MTTF + MTTR).

Reliability [R(t)]. R(t) is defined for a fixed time period to predict the number of devices that would perform reliably. It is cacluated from FIT and expressed as a percentage.

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